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Low Power Flip-Flop Grouping in Data-Driven Clock Gating

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Abstract

The increasing demand of digital component is very high due to high computation for mobile communication and different area of technology. The size of component and power consumption is major issue. Now a day's various authors and scientist used different model for data driven. The process of data driven mainly depends on the grouping of flip flop and latches. In this paper design low power consumption trigging gate for the processing of data. Data driven clock, bypass two bit of same timing constraints so that much of the timing path which repeated to the single data driven reduces calculation. Some of the default parameter of VLSI such as default offset after out for clock, default period analysis is most probably fixed and those are not having much variation. The design model simulates in Xilinx software. And validated the result in different set of grouping of bit.

Keywords: - ***Data Driven, Grouping of Flip-Flop, Clock Getting.***

INTRODUCTION

Now a day the increasing demands of electronics device and component in the field of mobile communication and data transmission device need a low power consumption circuit and increase the life time of device. The reduction of the consumption of power is major issue in VLSI design technology. Now a day's various authors used various approach such as clock gating and algorithm approach [1,2]. The clock gating technique is better design way of data driven function for the processing of data design circuit. Clock gating is one of the most frequently used techniques in RTL to reduce dynamic power consumption without affecting the functionality of the design. One method involves inserting gating conditions in the RTL, which the synthesis tool translates to clock gating cells in the clock-path of a register bank [3,4]. This helps to reduce the switching activity on the clock network, thereby reducing dynamic power consumption in the design. Since the translation done by the synthesis tool is purely combinational, it is referred to as combinational clock gating. This transformation does not alter the behavior of the register being gated. data-driven clock gating, employed for FFs at the gate level, which is the most aggressive possible. The clock signal driving a FF is disabled when the FFs state is not subject to change in the next clock cycle [6,7]. Data-driven gating is causing area and power overheads that must be considered. In an attempt to reduce the overhead, it is proposed to group several FFs to be driven by the same clock signal, generated by oaring the enabling signals of the individual FFs. This may however, lower the disabling effectiveness. It is therefore beneficial to group FFs whose switching activities are highly correlated and derive a joint enabling signal. The optimal fan-out of a clock gate yielding maximal power savings is derived based on the average toggling statistics of the individual FFs, process technology, and cell library in use [8,9]. In general, the state transitions of FFs in digital systems depend on the data they process. The rest of paper discuss in section II Related work. In section III discuss design of flip-flop. in section IV discuss experimental result and finally discuss conclusion and future work in section V.

II. RELATED WORK

In this section discuss the related work in the field of clock gating and low power design of latches and flip-flop. Now a day's various authors used various compact design for flip-flop and latches for data driven processing.

[1] According to researcher, Clock gating is a predominant technique used for power saving. It is observed that the commonly used synthesis-based gating still leaves a large amount of redundant clock pulses. Data-driven gating aims to disable these. To reduce the hardware overhead involved, flip-flops (FFs) are grouped so that they share a common clock enabling signal. The question of what is the group size maximizing the power savings is answered in a previous paper. Here they answer the question of which FFs should be placed in a group to maximize the power reduction. They discuss a practical solution based on the toggling activity correlations of FFs and their physical position proximity constraints in the layout. They described the problem of grouping FFs for joint clocking by a common gater to yield maximal dynamic power savings.

They discussed research work presents novel sub word partitioned signal range based clock gating technique,

which can be very efficient in signal processing applications. A scalable VHDL model is developed for the Correlator architecture with the proposed clock gating scheme. MATLAB script generated test data is used for functional verification. Xilinx FPGA based synthesis and power analysis tools are employed to analyze the power optimization of proposed architecture. Finally, they discussed, the signal width is divided into sub words where each subword is enabled with separate clock gating signal. The relationship between clock gating signals of adjacent sub words is fully utilized in realizing area efficient clock gating scheme. By reducing the area overhead for clock gating logic, the penalty on increased static and leakage power is less when compared to the saved dynamic power.

[3] They discussed the redundant clock pulses in a high frequency clock signal are eliminated by performing AND operation on Enable signal and applied clock signal. Enable signal is determined by performing XOR operation on input and output of sequential element such as Flipflop. and output the Gated clock signal serves as clock to the existing circuit, which consists of clock pulses at the switching activities of input signal. This method can be extended to group of Flipflops having similarly switching inputs by performing OR operation on the enable signals of all Flipflops in the group.

[4] They present a comparative analysis of existing clock gating techniques on some synchronous digital design like ALU (Arithmetic logical unit) etc. A new clock gating technique that provides more immunity to the existing problem in available technique. In new discussed clock gating the Gated Clock Generation Circuit is using tri state buffer and Gated logic is used which is created by the combination of double gated (AND, OR, AND logic gate) with bubbled input respectively. This circuit saves power even when Target device's clock is ON. All experiments are done on Xilinx14.1 EDA tool. Mentor Graphics Model SIM. For power calculation they are using XPOWER. Sparten-3 (90nm) FPGA platform is used for result and analysis.

[5] They described, the auto gated flip-flops which are to be using clock gating technique for only small power consumption. The novel approach they are going to design the circuit based on look ahead clock gating which is to be used for the timing constraints for each clock pulses. The enabling clock pulses for the derived timing signals to the gated logic which is to be saves the power from the flip-flops. The look ahead technique can also to be reducing the delay and the distortions from the circuit for the achievement of the application level. This could be applied into the parallel bus specific clock gating for application level implementation.

[6] They describe VLSI and other electronics industries has become imminent to address the three very basic issues namely speed, power and size. The main focus is on the power parameter. Generally synchronous circuits waste a lot of clock pulses. This means that the pulses are consumed even if the output is not changing. It is seen that the one of the major sources of power dissipation is wastage of clock pulses. In this implantation clock gating technique is used to reduce power consumption as compared to non-gated circuit. According to author, the problem of dynamic power dissipation is addressed. It is observed that the dominant source of dynamic power dissipation is by unnecessary clocking in circuits. A register bank containing D flip-flops subjected to clock gating is simulated and its output in the form of waveform is achieved.

[7] They have implemented different type of clock gating techniques and proposed technique to reduce power. All the techniques are performed at different technology with temperature, voltage and frequency variation and their Dynamic, static and total power has been computed, they are applying clock gating techniques on a 8 bit Arithmetic logical unit (ALU). Here they had compared different clock gating techniques i.e without clock gating, and gate based, latch based, mux based, flip flop based, positive level sensitive latch based, T-FF based, double gated based, negative latch based with their discussed clock gating technique.

[8] Author describes the design method is needed that consume less power while maintaining the comparable performance method. Power consumption is the conventional CMOS digital circuit can be separated into three types of power dissipation:(i) switching power, (ii) short-circuit power, and (iii) leakage power consumption. A new technique is discussed based on the comparison between Conventional Transistorized Flip flop and Data transition Look ahead D flip flop here they are checking the working of DLDFF and the conventional D Flip-flop after that they are analyzing the characteristic comparison using power & area constraints after that they are proposing a Negative Edge triggered flip-flop named as Switching Transistor based D Flip-Flop (STDFF) with reduced number of transistors which will reduce the overall power area as well as delay. The simulation is done by using Tanner EDA analysis software tools and the result between all those types is under 130 nm technology.

[14] Author introduces a novel Look-Ahead Clock Gating (LACG) method which is the combination of all the three gating methods. It calculates the clock enabling signals of every flip flops one cycle from this time, which it depends on the FFs cycle data at present. In a CPU, the most commonly edited modules are the ALU. During most instruction executions, it is employed. Therefore, a major concern in the ALU is the consumption of power. They motivate to reduce the ALU architecture for many digital applications and to improve the internal process in ALU architecture with look ahead clock gating approach. Finally, they discussed a low power look ahead clock gating is presented and compared it with the previously clock gating technique i.e. the data driven

clock gating and with clock. It is also very useful in reducing the dynamic power. One of the major sources responsible for power consumption in digital circuits is the systems clock signal. It contributes towards a large amount of power consumption.

III. FLOW DESIGN OF FLIP-FLOP

Working of multi-bit D flip flop is similar to the D latch except that the output of D Flip Flop takes the state of the D input at the moment of a positive edge at the clock pin and delays it by one clock cycle. That's why, it is commonly known as delay flips flop[5]. The D Flip-Flop can be interpreted as a delay line or zero order hold. The advantage of the D flip-flop over the D-type transparent latch is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. From the timing diagram in fig 1 it is clear that the output Q changes only at the positive edge. At each positive edge the output Q becomes equal to the input D at that instant and this value of Q is held until the next positive edge[15].

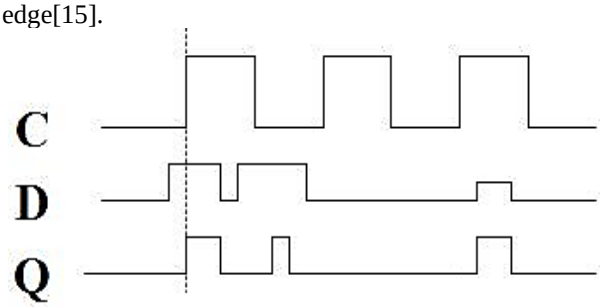

Figure 1: shows that clock time diagram for clock gating

Data driven Flip Flop which takes multiple data input and results in multiple data output. The working of multi-bit flip flop is same as single-bit flip flop, whenever the clock gets active state flip flop latches all input to output. For inactive state the flip flop holds the data. The basic structure of data driven flip flop is given in figure 4.4. 2 and its corresponding waveform is given in figure4.4.3.

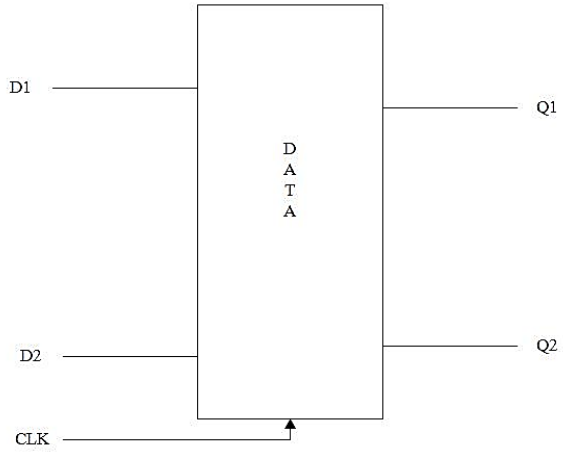

Figure 2: shows that data driven FFs

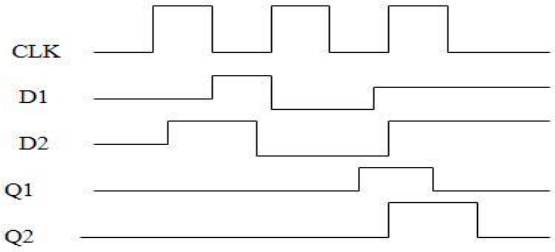

Figure 3: shows that clock input of FFs

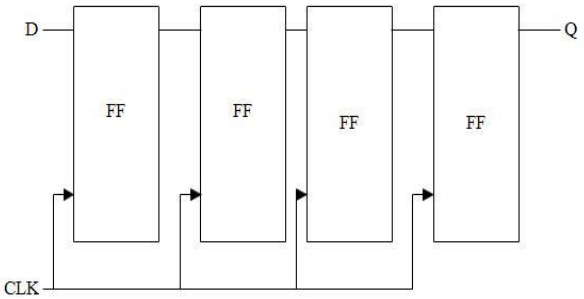

Figure 4: shows that grouping of FFs for clock gating

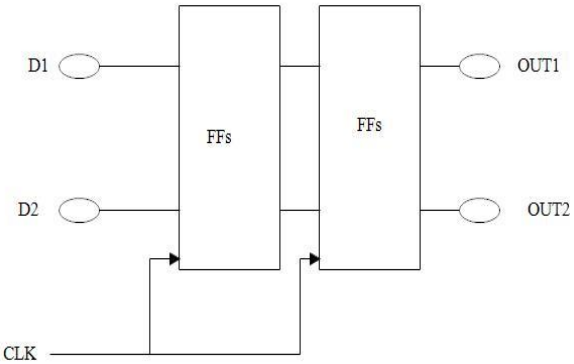

Figure 5: shows that grouping of FFs for clock gating with input group flip-flop and output clock gate.

Algorithm Functional Component Placement in FFs
Given the execution trace and the set of functional components

step 1: obtain instruction execution frequency, IF;

step 2: obtain the functional component execution frequency based on IF;

step 3:

/* Find the location for each component in the chain*/ /* Start from the closest level to the output */current level = 1;

/* If there are more than 2 components in FC */**while** |FC| > 2 **do**

S<= most frequent components in F C; FC <= FC − S;

/* Repeat if there are multiple such components */

while S = φ **do**

get the component of highest weight, fc in S; /* Assign the component to the current level */level(fc)= current level;
/* Go to one level further from the output */current level ++;
S<= S − fc;
end while

.

IV. EXPERIMENTAL ANALYSIS

In this section discuss the design and simulation of proposed model of clock gating for grouping of FFs architecture for the processing of reduction of power consumption. The design data driven simulate in Xilinx software. The Xilinx software version is 12.1.

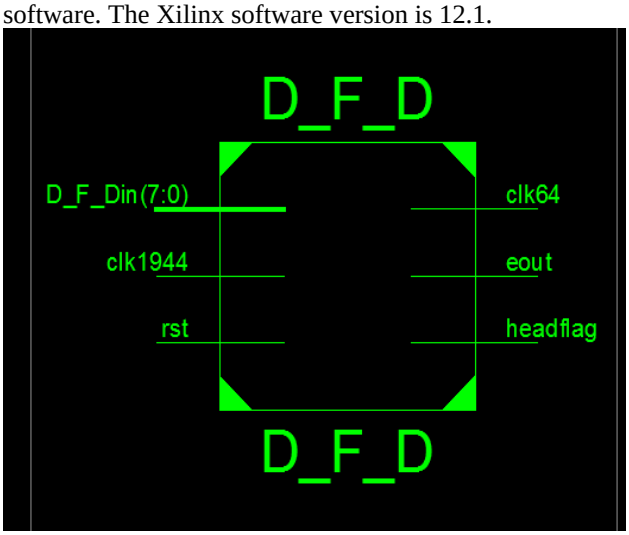

Figure 6: Shows that the parameter being used in a implementation phase will contain the logic gates.

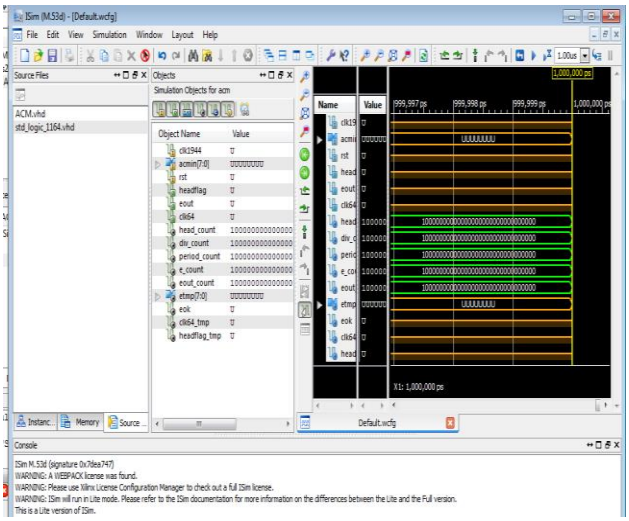

Figure 7: Shows that the all implementation parameter values for the DFD 2 files used in implementation phase with logic utilization value and number of flip flop values.

Local Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip-Flops	143	1536	9%
Number of 4 Input LUTs	268	1536	17%
Number of Occupied files	210	768	27%
Number of Slices Containing only related logic	210	210	100%
Number of Slices Containing only unrelated logic	0	210	0%
Total Number of 4Input LUTs	402	1536	26%
Number used as logic	268		
Number of Bonded	13	124	10%
Number of BUFGMUXs	2	8	25%

Table 1: Shows that the Utilization value of used and available parameter for the experimental process in a simulation model.

Local Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip-Flops	170	1864	10%
Number of 4 Input LUTs	324	1864	21%
Number of Occupied files	260	838	33%
Number of Slices Containing only related logic	260	260	100%
Number of Slices Containing only unrelated logic	0	260	0%
Total Number of 4Input LUTs	445	1536	29%
Number used as logic	324		
Number of Bonded	19	138	16%
Number of BUFGMUXs	6	12	34%

Table 2: Shows that the Utilization value of used and available parameter for the experimental process in a simulation model.

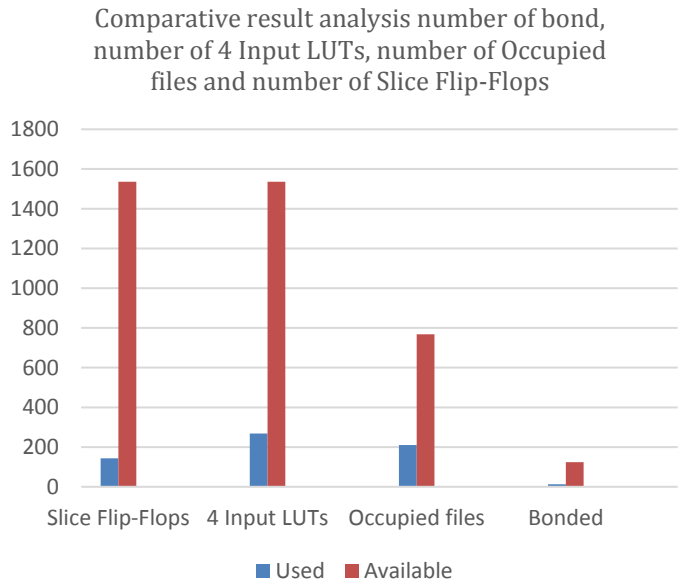

Figure 8: shows that comprative result analysis of number of bond, number of 4 Input LUTs, number of Occupied files and number of Slice Flip-Flops in Logic Utilization.

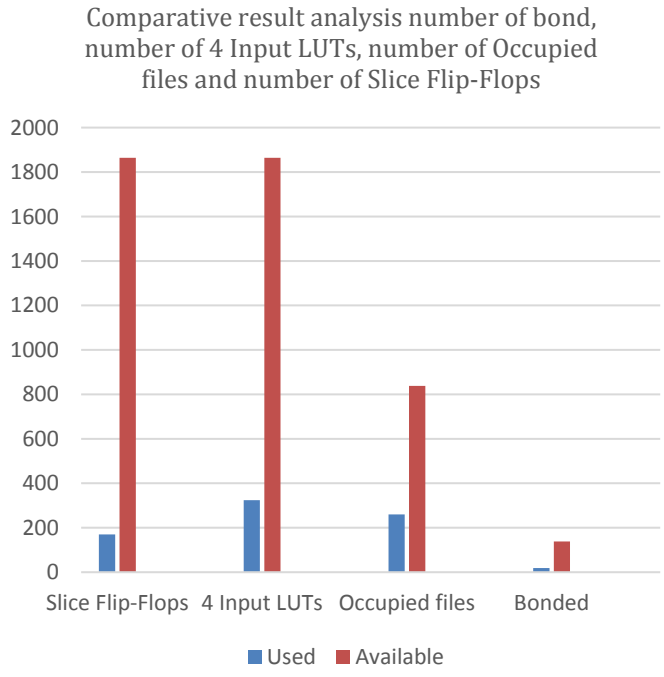

Figure 9: shows that comprative result analysis of number of bond, number of 4 Input LUTs, number of Occupied files and number of Slice Flip-Flops in Logic Utilization.

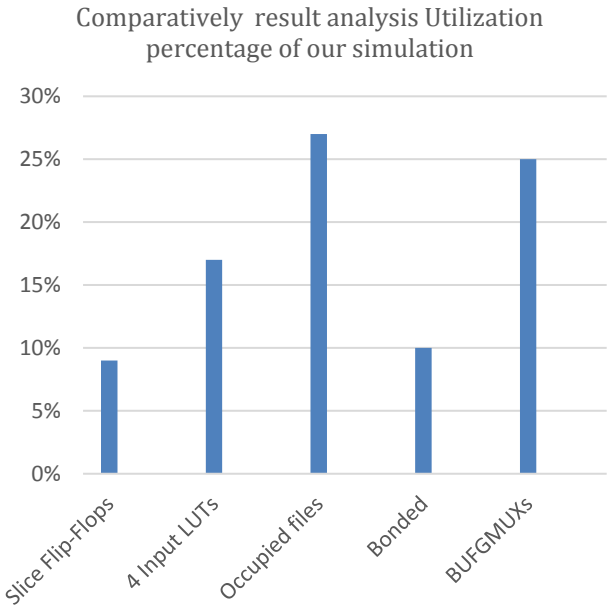

Figure 10: shows that comprative result analysis of utilization for number of slice flip flops, number of 4 input LUTs, number of occupied files number of bonded and number of BUFGMUXs in Logic Utilization simulation.

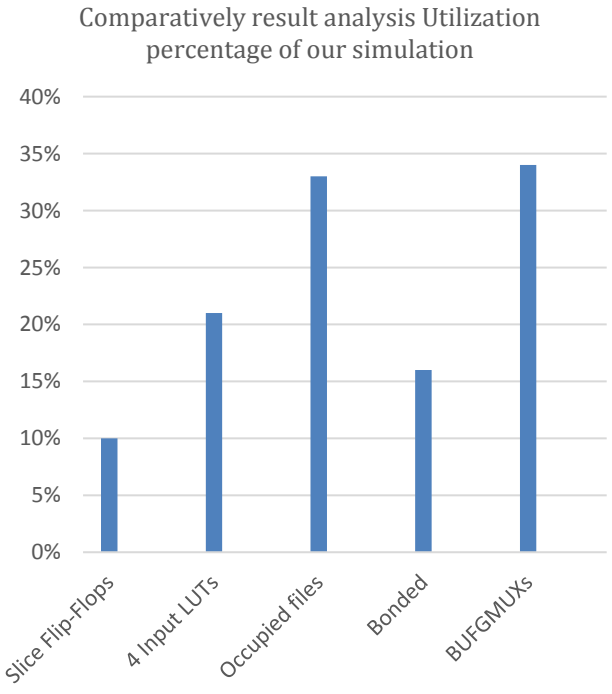

Figure 11: shows that comprative result analysis of utilization for number of slice flip flops, number of 4 input LUTs, number of occupied files number of bonded and number of BUFGMUXs in Logic Utilization simulation.

V. CONCLUSION & FUTURE SCOPE

Our proposed technique reduces the designer's difficulty for analyzing all the flip-flops for meeting the timing requirements. Data driven clock, bypass two bit of same timing constraints so that much of the timing path which repeated to the single data driven reduces calculation. Some of the default parameter of VLSI such as default offset after out for clock, default period analysis is most probably fixed and those are not having much variation. This proposed method is implemented in Xilinx Virtex 5 VLSI family. Experimental results are targeted to number of flip flop usage, delay and clock buffer. Flip flop area usage is minimized approximately to 50%. Thus, this proposed method is more suitable for reduction of hardware. The design of data driven clock gating system using AND or NOR with the combination of Latch based clock gating system. The clock gating system used BAN network for clock distribution and reduces the consumption of power. In future used lower level clock gated input for optimization of power.

References

[1] Shmuel Wimer and Israel Koren "Design Flow for Flip-Flop Grouping in Data-Driven Clock Gating", IEEE, 2014, Pp 771-778.
[2] A. Ranganayakulu and K. Satyaprasad "Low Power Correlator Using Signal Range and Sub Word Based Clock Gating Scheme", International Journal of Hybrid Information Technology, 2016, Pp 159-170.
[3] T.Naresh and M.Lakshmi Kiran "Power Reduction with FlipFlop Grouping in Data Driven Clock Gating", International Journal Of Engineering And Computer Science, 2015, Pp 11835-11838.
[4] Dushyant Kumar Soni and Ashish Hiradhar "Dynamic Power reduction of synchronous digital design by using of efficient clock gating technique", International Journal of Engineering and Techniques, 2015, Pp 18-23.
[5] Vidya K and Mr R. Karthik "a look ahead partial bus specific clock gating based on autogated flipflops", International Journal of Research in Science and Engineering, 2015, Pp 1-7.
[6] Saurabh Kshirsagar and Dr. M B Mali "Data Driven Clock Gating for Logical Groups in Low Power Applications", IJESC, 2015, Pp 1454-1457.
[7] Renuka Jaiswal, Ranbir Paul and Vikas Ranjan Mahto "Power Reduction in CMOS Technology by using Tri-State Buffer and Clock Gating", IJARCET, 2014, Pp 1853-1860.
[8] R Dhivya Bharathi and M Sunil Karthik "a pass transistor based d flip-flop design using negative edge triggered circuit", IJERST, 2015, Pp 63-69.

[9] S Chindhu and S Thenappan "Pass Transistor Based Conventional Data Flip Flop Design", IJERST, 2015, Pp 278-284.
[10] Kakarla Sandhya Rani and Krishna Prasad Satamraju "A Novel Approach for Auto Clock Gating of Flip-Flops", IJSER, 2015, Pp 132-136.
[11] Anuja Aravind and Raseena K.A "Design of an ALU with a low power LFSR using Clock gating", IJSETR, 2014, Pp 2636-2639.
[12] Abhishek Mashetty, Rajashekar Reddy Merugu, Sanjay Dubey and Vejandla Vijay Bhaskar "Data driven clock gating technique for dynamic power reduction in digital design", Journal of Chemical and Pharmaceutical Sciences, 2016, Pp 511-514.
[13] C.Subin Raj, S.Jebasing Kirubakaran and P.Bala Vengateswarlu "Look Ahead Clock gating using an Auto gated Flip flop for Low Power Application", Journal of Chemical and Pharmaceutical Sciences, 2016, Pp 969-973.
[14] D.Nirosha and T.Thangam "Design and Implementation of 32 Bit ALU Using Look Ahead Clock Gating Logic", IJETER, 2016, Pp 101-104.
[15] Shmuel Wimer and Arye Albahari "A Look-Ahead Clock Gating Based on Auto-Gated Flip-Flops", IEEE, 2014, Pp 1465-1472.