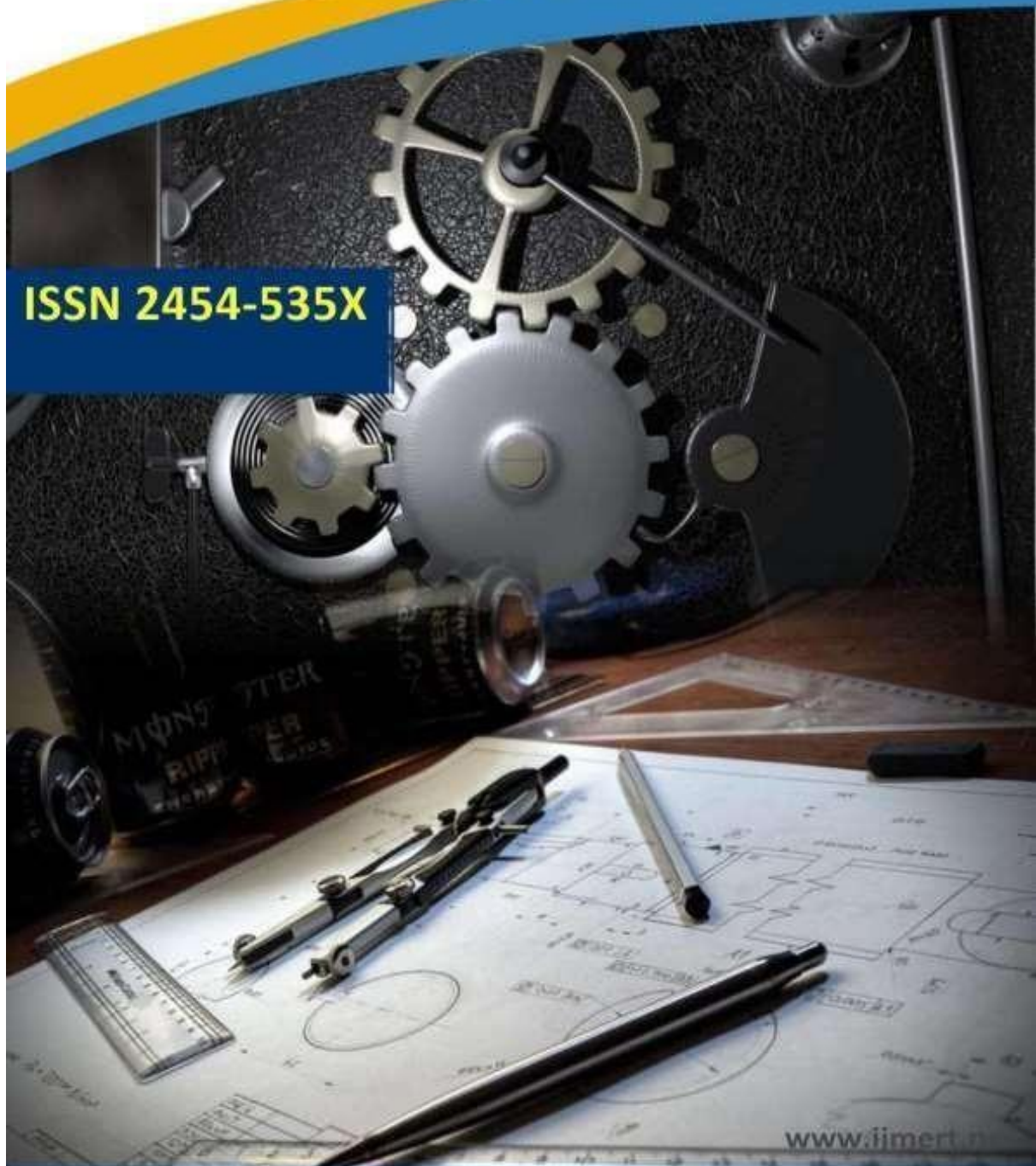




International Journal of Mechanical Engineering Research and Technology

ISSN 2454-535X



Email ID: info.ijmert@gmail.com or editor@ijmert.net



DESIGN A HIGH-PRECISION VLSI ARCHITECTURE OF RECONFIGURABLE FFT PROCESSOR

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ABSTRACT: In this paper the design a high-precision VLSI architecture of reconfigurable FFT processor is implemented. Basically the FFT supports the bit size which is suitable to the system and mostly used in the long term evolution systems. Transport triggered architecture is utilized to customize the size of fault free FFT processor. Here the both energy-efficiency and performance is evaluated by using the standard cell technology. Computing address unit generates the address to access the main memory. Barrel shifter is used to shift the position of bits. Data merging block will merge the bits very effectively. All the shifter data and merged data is saved in the data memory blocks. Memory access controller will control the data while accessing to the reconfigurable unit. Twiddle factor is used to speed the operation of system. At last from simulation result it can observe that reconfigurable FFT processor gives effective outcome.

KEY WORDS: FFT, Data merger, Barrel shifter cluster, Memory Access controller, Twiddle factor.

I. INTRODUCTION

Generally, discrete Fourier transform is introduced in 1965. Basically, the discrete Fourier transform is taken from the fast Fourier calculation. All things considered, after practically 50 years, stays extremely high because of key helpful properties of DFT. The ongoing increase in such intrigue is because of correspondence applications, specifically Long Term Evolution (LTE) and Software Defined Radio (SDR) [1]. In these applications, productive usage of DFT are required so as to help very tight, commonly negating limitations, for example, hard ongoing necessities over low-control, Minimal effort and adaptable HW stages. In the OFDM images using the Discrete Fourier to obtain the high speed operation in the system.

Here the length of each image is considered as N and these produces complex quantities in the entire system. Hence the vector image is used with the length of $N = 128$. In the Meantime, the plan eases to be valuable and the primary target gadgets are compact purchaser Electronics, for example, portable (advanced cells,) workstations, and so forth. Then again, plans of action require adaptable programmable usage [2].

Basically, the main intent of filters is to use partial range of frequency to emphasize the signals. But here the signals are getting rejected because of selection of frequency range in alternate way. Coming to the designing part of circuit, the frequency is selected alternatively. Here the frequency range is connected to the electric network. This electric network works depending on the characteristics of signals. The characteristic parameters are amplitude, frequency and time [3].

Depending on these parameters the entire electric network works. Here this may come to know that, there will be no change in allotted frequency and as well as cannot add new frequency to the system. Filters are mainly used in the applications of medical, automotive. There is a unity of region with some very surprising bases of characterization channels and these cover in some unique ways; there is no direct hierarchical grouping. As the social properties of the sign change, separation strategies will be considered. FFT is an elective calculation procedure for discrete Fourier change as it registers

rapidly. FFTs are utilized in countless applications extending from advanced sign preparing and furthermore in the calculations, for example, understanding the incomplete differential conditions, augmentation of enormous esteem whole numbers and so forth. FFT processor working recurrence decides the range for which the processor can be utilized. The processor is intended to figure countless complex increases both at rapid and withreliable throughput.

The other design challenges are found in the way in which, by changing the number of centers in FFT, the processor can be suitable for several applications that work both from the structure and from sensitive applications. Despite the way in which this is apparently useful, the fluctuation of the number of centers emphasizes different changes both at the registration level and through the change in the number of bits and the level of construction based on the variation in the length of the displacement registers, analogously to regulation of the meaning of ROM.

II. FFT PROCESSOR

The below figure (1) shows the architecture of FFT processor system. In the memory based FFT processor architecture is using two modules and this can performs fast operations without zero padding. Here radix architecture is shown and multipliers are used. All these components combine together and give the specified output.

In this memory based FFT processor system, for the purpose of modular reduction and conditional sequences are using the number of multiple operations units. Here the pipeline architectures are designed inside the each unit and the entire operation is performed sequentially. Next coming to the block butterfly unit, it performs the forward and inverse operation. In multiple adder

unit, the component wise multiplication and addition operations are performed. Now for the time domain operations are using the ripple carry adder, subtractor and shift module units. Control unit is used to generate the control signals in the system. Coming to memory, it consists of several RAM sets which stores the recomputed data and intermediate results.

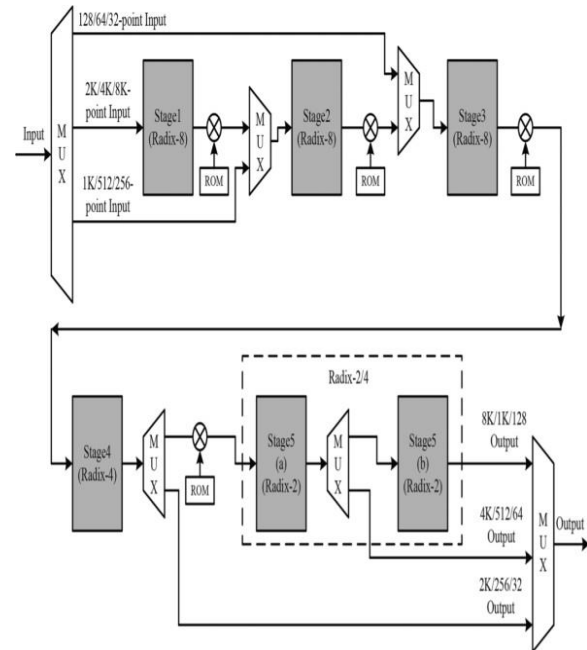


Fig. 1: FFT PROCESSOR

The first and principle significant part in the design is multiply and adder unit. This unit actualizes the segment insightful augmentation and expansion of FFT-RAM. To understand the segment savvy increase when operand size isn't bigger than couple of hundred bits then karatsuba technique is utilized. The multiplier and adder units works with pipeline of 3 bit data sources and one piece yield. Finally to improve the presentation of increase, karatsuba strategy is connected recursively. This is about duplicate and snake unit and let us examine about FFT unit.

Next it is connected to FFT calculation. The principle correlation of set up and consistent geometry FFT is it has same association arrange between each neighboring stages.

The FFT is structured with six data sources. In this the four contributions forward the digits into BFSs for FFT calculation and the other two contributions forward the pre-registered upper bound imperatives into FSO.

III. RECONFIGURABLE MEMORY BASED FFT

The below figure (2) shows the blockdiagram of proposed system. Data merging block will merge the bits very effectively. All the shifter data and merged data is saved in the data memory blocks. Memory access controller will control the data while accessing to the reconfigurable unit. Twiddle factor is used to speed the operation of system.

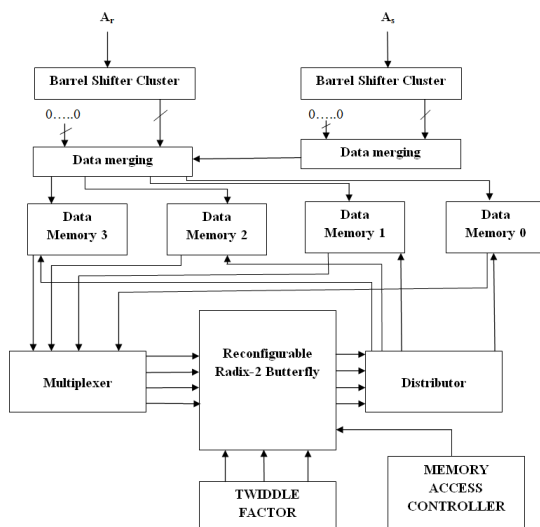


Fig. 2: RECONFIGURABLE MEMORY BASED FFT PROCESSOR

A Fast Fourier Transform (FFT) is an estimate that represents the Discrete Fourier Transform (DFT) of a meeting or its round (IDFT). Fourier's examination changes on a sign of this extraordinary region(occasionally time or space) to arepresentation in the space of repetition and in a different way. DFT is obtained by breaking down a progression of characteristics in different frequency portions. This action is important in several fields, but its direct management from the

definition is as frequent as possible, excessively moderate or possibly conventional.

Radix butterfly unit, is an execution unit inside Control Processing Units (CPUs) that ascertains addresses utilized by the CPU to get to primary memory. By having address estimations taken care of by discrete hardware that works in parallel with the remainder of the CPU, the quantity of CPU cycles required for executing different machine directions can be diminished, bringing execution upgrades. While performing different tasks, CPUs need to compute memory tends to required for bringing information from the memory; for instance, in-memory places of exhibit components must be determined before the CPU can get the information from genuine memory areas. Those location age computations include distinctive number-crunching tasks, for example, expansion, subtraction, modulo activities, or bit shifts.

The technique that is utilized to exchange data between inward capacity and outer gadgets is known as I/O interface. The CPU is interfaced utilizing unique correspondence interfaces by the peripherals associated with any PC framework. These correspondence connections are utilized to determine the contrasts among CPU and fringe. There exists extraordinary equipment parts among CPU and peripherals to administer and synchronize all the info and yield exchanges that are called interface units.

Twiddle factors are utilized in direct current (DC) machines: dynamos (DC generators) and numerous DC engines just as widespread engines. In an engine the commutator applies electric flow to the windings. By switching the present bearing in the pivoting windings every half turn, a consistent pivoting power (torque) is delivered. At least two electrical contacts

called "brushes" made of a delicate conductive material like carbon press against the commutator, reaching progressive sections of the commutator as it pivots. The windings (loops of wire) on the armature are associated with the commutator portions.

IV. RESULTS

The below figure (3) shows the RTL schematic of proposed system.

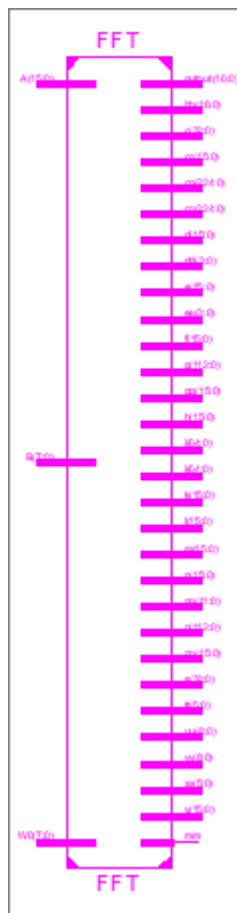


Fig. 3: RTL SCHEMATIC

The below figure (4) shows the technology schematic of proposed system.

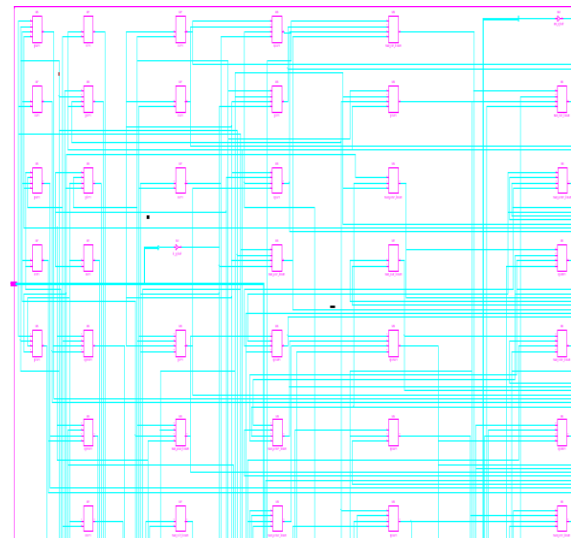


Fig. 4: TECHNOLOGY SCHEMATIC

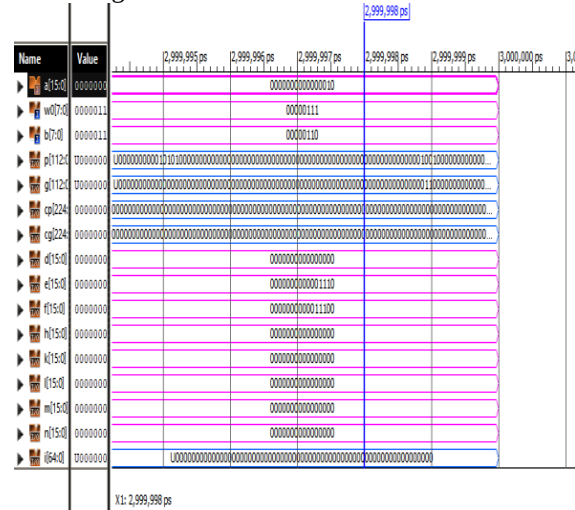


Fig. 5: OUTPUT WAVEFORM

V. CONCLUSION

Hence in this paper design high-precision VLSI architecture of reconfigurable FFT processor was implemented. In present day sign preparing circuits, it is entirely expected to discover a few channels working in parallel. Reconfigurable memory based FFT processor framework is a zone productive system to identify and address single mistakes. Data merging block will merge the bits very effectively. All the shifter data and merged data is saved in the data memory blocks. Memory access controller will control the data while accessing to the reconfigurable unit. Twiddle factor is used



to speed the operation of system. At last from simulation result it can observe that reconfigurable FFT processor gives effective outcome.

VI. REFERENCES

- [1] Yu Xie, Chen Yang, Chuang-An Mao, He Chen and Yi Zhuang Xie, “A Novel Low-Overhead Fault Tolerant Parallel Pipelined FFT Design”, 978-1-5386-0362-8/17/\$31.00 2017 □ IEEE.
- [2] Syed M. A. H. Jafri, Stanisław J. Piestrak, Kolin Paul, Ahmed Hemani, Juha Plosila, and Hannu Tenhunen, “Energy-Aware Fault-Tolerant CGRAs Addressing Application with Different Reliability Needs”, 978-1-4661-7131-3/\$26.00 © 2013 IEEE.
- [3] Abbas BanaiyanMofrad, Housman Homayoun, Nikil Dutt, “FFT-Cache: A Flexible Fault-Tolerant Cache Architecture for Ultra Low Voltage Operation”, CASES’11, October 9–14, 2011, Taipei, Taiwan.
- [4] C. Radha krishnan and W. K. Jenkins, “Fault Tolerant Adaptive Filters Based on Modified Discrete Fourier Transform Architectures”, 978-1-4244-9474-3/11/\$26.00 © 2011 IEEE.
- [5] Hongyi Fu, Xuejun Yang, “Fault Tolerant Parallel FFT Using Parallel Failure recovery”, 978-0-7695-3701-6/09 \$25.00 © 2009 IEEE.
- [6] Jin-Fu Li, Shyue-Kung Lu, Shih-Arn Hwang, “Easily Testable and Fault-Tolerant FFT Butterfly Networks”, 1057–7130/00\$10.00 © 2000 IEEE.
- [7] G. Robert Redinbo, Ranjit Manomohan, “Fault-Tolerant FFT Data Compression”, 0-7695-0975-4/00 \$10.00 © 2000 IEEE.
- [8] Jin-Fu Li and Cheng-Wen Wu, “Testable and Fault Tolerant Design for FFT Networks”, 2000 IEEE Conference.
- [9] Shyue-Kung Lu, Cheng-Wen, Wu Sy-Yen Kuo, “On Fault-Tolerant Fft Butterfly Network Design”, 0-7803-3073-0/96/\$5.00 © 2000 IEEE.

- [10] Bernard A. Schnauffer and W. Kenneth Jenkins, “A Fault Tolerant FIR Adaptive Filter Based on the FFT”, 0-7803-1775-On4 \$3.00 © 1994 IEEE.