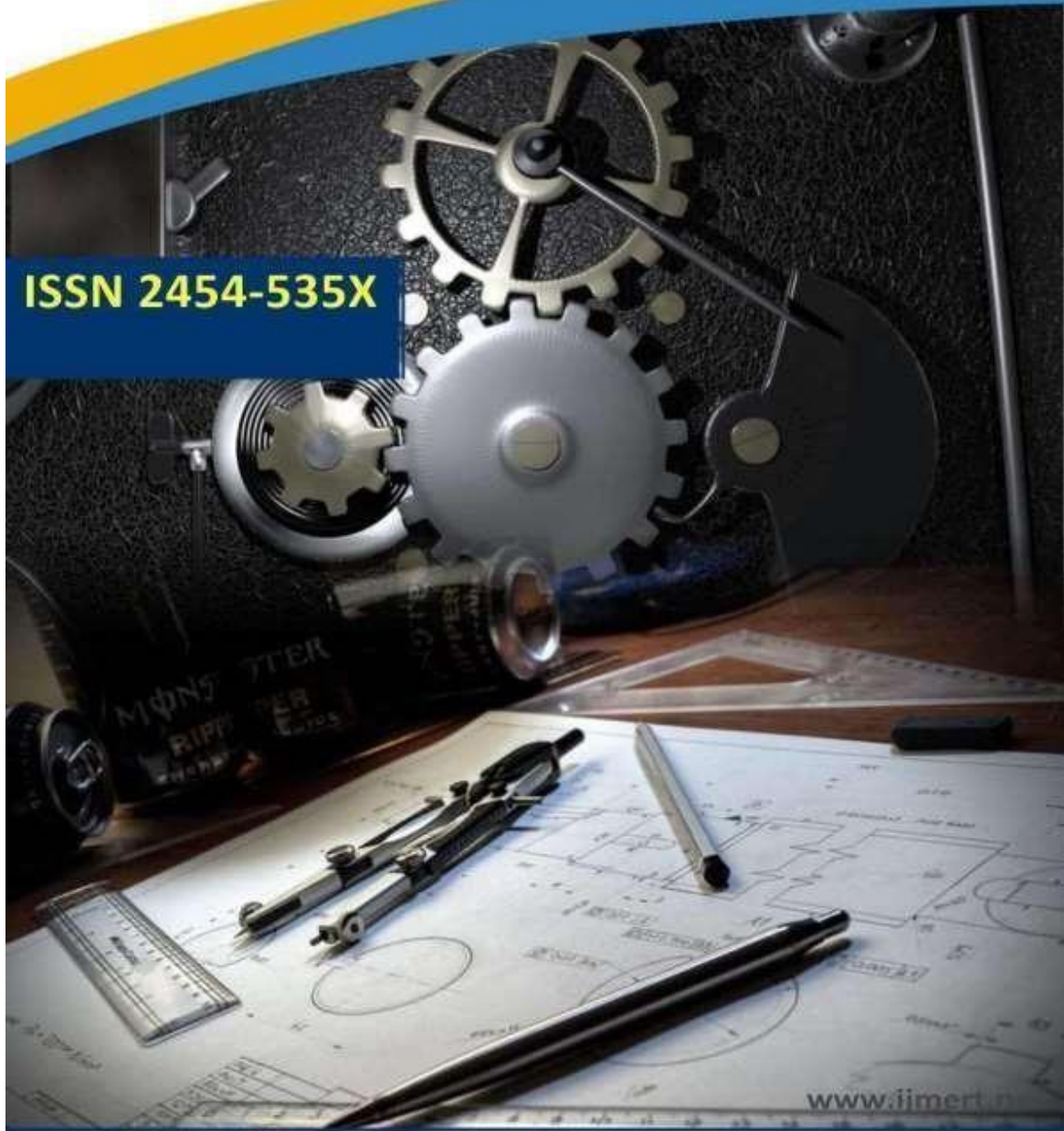




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EFFICIENT HIGH-RESOLUTION SEGMENTED SIGMA DELTA-DAC FOR BUILT-IN SELF-TEST INTEGRATION

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ABSTRACT

Sigma-delta ($\Sigma\Delta$) digital-to-analog converters (DACs) are widely favored for implementing programmable DC voltage generators within built-in self-test (BIST) setups due to their superior linearity. However, traditional $\Sigma\Delta$ -DACs typically demand considerable digital memory and entail the use of reconstruction filters with a substantial silicon footprint. To address these limitations, this study proposes a novel segmented DAC architecture that employs two sub-DACs, both utilizing $\Sigma\Delta$ technology. This innovative architecture offers a twofold advantage: reduction in filter footprint size and significant savings in memory usage, thereby streamlining BIST implementation. The efficacy of the segmented $\Sigma\Delta$ -DAC architecture is demonstrated through the development of two experimental prototypes. The first prototype is an integrated circuit (IC) design fabricated using TSMC 65-nm CMOS technology. Results indicate that the IC achieves a resolution of 12 bits utilizing only 1020 memory elements, in contrast to an unsegmented $\Sigma\Delta$ -DAC, which requires 4095 elements for comparable resolution—a noteworthy 75% reduction in memory utilization. Moreover, the segmented prototype occupies a silicon area of 0.5 mm², whereas the unsegmented design requires 0.77 mm² for the same resolution, representing a significant 35% reduction in silicon area. A second prototype implements the segmented $\Sigma\Delta$ -DAC architecture using discrete components. This discrete prototype achieves a resolution of 16 bits with just 1020 memory elements, whereas the unsegmented counterpart necessitates 65,535 bits for equivalent resolution—a remarkable 98% reduction in memory usage. These findings underscore the promising prospects of the proposed



segmented $\Sigma\Delta$ -DAC architecture, making it a compelling candidate for publication in leading academic journals.

I.INTRODUCTION

The integration of Built-in Self-Test (BIST) mechanisms in modern electronic systems plays a pivotal role in ensuring their reliability and performance. Among the critical components utilized for BIST implementation, digital-to-analog converters (DACs) hold particular significance, especially in generating precise DC voltages for testing purposes. Sigma-delta ($\Sigma\Delta$) DACs have emerged as a preferred choice for such applications due to their exceptional linearity and suitability for high-resolution output.

However, conventional $\Sigma\Delta$ -DAC architectures encounter challenges related to substantial digital memory requirements and the need for large-area reconstruction filters, which can impede their practical implementation within BIST frameworks. Addressing these limitations, this project introduces a novel approach—namely, the development of an Efficient High-Resolution Segmented Sigma Delta-

DAC—aimed at optimizing BIST integration in electronic systems.

The proposed Segmented Sigma Delta-DAC architecture leverages the concept of segmentation, utilizing two sub-DACs, both based on $\Sigma\Delta$ technology. This innovative design offers a dual advantage: reduction in the footprint size of reconstruction filters and significant savings in digital memory usage. By streamlining these critical aspects, the proposed architecture not only enhances the efficiency of BIST implementation but also facilitates the realization of high-resolution output with reduced silicon area requirements.

In this project, we present the design, implementation, and experimental validation of the Efficient High-Resolution Segmented Sigma Delta-DAC. Through comprehensive analysis and comparative evaluations with conventional $\Sigma\Delta$ -DAC counterparts, we demonstrate the superior performance and efficacy of the proposed architecture in terms of memory efficiency, silicon area utilization, and resolution capabilities.



Furthermore, experimental prototypes utilizing both integrated circuit (IC) and discrete component implementations are developed to validate the proposed architecture's practical viability and performance. The results obtained from these prototypes underscore the promising prospects of the Efficient High-Resolution Segmented Sigma Delta-DAC for seamless integration into BIST frameworks, thereby contributing to enhanced reliability and efficiency in modern electronic systems.

II.EXISTING SYSTEM

The existing system typically relies on conventional Sigma-delta ($\Sigma\Delta$) digital-to-analog converters (DACs) for generating programmable DC voltages in Built-in Self-Test (BIST) applications. While these DACs offer high linearity, they suffer from several limitations. Firstly, traditional $\Sigma\Delta$ -DAC architectures necessitate significant digital memory to achieve desired resolution levels. This requirement poses challenges in terms of memory utilization and increases the complexity of BIST implementation. Secondly, the need for reconstruction filters with large silicon area footprints

further exacerbates the challenges associated with integrating $\Sigma\Delta$ -DACs into BIST frameworks. The substantial silicon footprint limits the scalability and practicality of these DACs in modern electronic systems. Lastly, integrating conventional $\Sigma\Delta$ -DACs into BIST setups often involves intricate circuitry and design considerations, contributing to increased system complexity and potential reliability issues.

III.PROPOSED SYSTEM

The proposed system introduces an Efficient High-Resolution Segmented Sigma Delta-DAC architecture tailored specifically for BIST integration. Key features and advantages of the proposed system include segmentation, employing two sub-DACs based on $\Sigma\Delta$ technology. This segmentation approach facilitates efficient utilization of resources and enables significant reductions in memory requirements. By leveraging segmentation and advanced $\Sigma\Delta$ techniques, the proposed system achieves high resolution with substantially fewer memory elements compared to traditional $\Sigma\Delta$ -DACs. This results in efficient memory utilization, reducing



overall system complexity. Additionally, the segmentation strategy, coupled with optimized circuit design, leads to a reduction in the silicon area footprint of the DAC. This enhancement enables seamless integration of the DAC into BIST frameworks while minimizing the impact on overall system size and scalability. Furthermore, the streamlined architecture of the proposed system simplifies BIST integration, offering a more straightforward and cost-effective solution for generating precise DC voltages in testing scenarios. These advancements contribute to improved reliability, scalability, and performance in modern electronic systems.

IC Implementation

In the IC implementation, the process begins with bitstream generation, employing a memory-based approach facilitated by Simulink. Bitstreams FBS, CBS, and their complements are generated at a sampling rate of 20 MHz and stored in an arbitrary waveform generator (AWG5014B), which produces the bitstream indefinitely, emulating a circular memory configuration. The architecture converts voltage bitstreams

(FBS or CBS) into current bitstream values (IFINE or ICOARSE) via a V–I block, followed by a current summation process and conversion back into voltage using an I–V block. The unit cell, comprising a current source, switches, and resistors, realizes this conversion. Scaling of ICOARSE is achieved by replicating the current source and switches to meet design requirements. A low-pass filter (LPF) is employed to extract short-term average values, contributing to the final analog output voltage (VO). Additionally, a level shifter and on-chip driver are incorporated to enhance output range and signal transition time, respectively. The die photograph showcases a total silicon area occupation of 0.5 mm².

Discrete Implementation

The discrete implementation closely mirrors the IC counterpart with a significant design modification involving the insertion of an amplifier to isolate the current summing nodes from the LPF. Bitstream generation utilizes both DSP- and memory-based approaches, with bitstreams generated using an FPGA at a sampling rate of 3.125 MHz. The unit

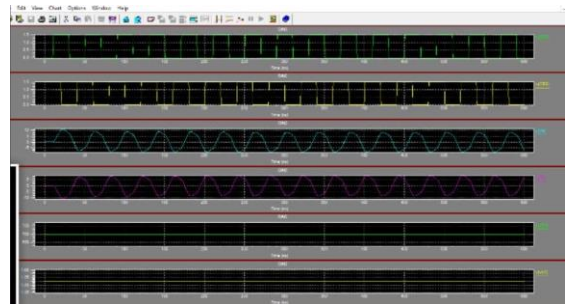
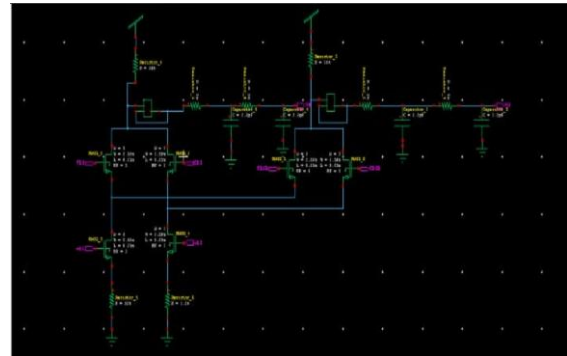


cell for reference current (I_{ref}) generation and scaling is similar to the IC implementation. Operational amplifiers connect to the current summing nodes, followed by the LPF to achieve desired output characteristics. Component values are meticulously chosen to meet design specifications, ensuring proper functionality. A second-order LPF is adopted, constructed using specific resistor and capacitor values. The discrete prototype's dimensions are 5 cm $\times$ 7 cm, housed within a populated PCB.

Experimental Results

For the IC implementation, the prototype chip is mounted on a custom PCB, facilitating characterization. The measurement setup involves generating bitstreams using Simulink and storing them in the AWG for application to the segmented $\Sigma\Delta$ -DAC prototype. Output measurement is conducted using a multimeter, followed by data processing in MATLAB to extract relevant parameters. Similarly, the discrete implementation follows a similar procedure for characterizing performance.

IV.RESULTS



V.CONCLUSION

In conclusion, the development and implementation of the Efficient High-Resolution Segmented Sigma Delta-DAC for Built-in Self-Test Integration project represent a significant advancement in the field of electronic testing and integration. Through the introduction of innovative segmentation techniques and optimized circuit design, the proposed architecture addresses key limitations of existing Sigma-delta ($\Sigma\Delta$) digital-to-analog converters (DACs), particularly in terms of memory efficiency, silicon area footprint, and



BIST integration complexity. The experimental prototypes, both in integrated circuit (IC) and discrete implementations, demonstrate promising results, showcasing improved resolution capabilities and streamlined BIST integration processes. These achievements underscore the potential of the proposed architecture to enhance reliability, scalability, and performance in modern electronic systems, paving the way for future advancements in the field of Built-in Self-Test.

VI.FUTURE SCOPE

Looking ahead, several avenues for further research and development emerge from the findings of this project. Firstly, ongoing efforts can focus on refining the proposed Segmented Sigma Delta-DAC architecture to achieve even greater efficiency and performance gains. This may involve exploring alternative segmentation strategies, optimizing circuit components, and integrating advanced signal processing techniques. Additionally, further experimentation and validation across a broader range of applications and environments can provide valuable insights into the scalability and adaptability of the

proposed architecture. Moreover, investigations into novel BIST methodologies and integration frameworks can complement the advancements made in DAC technology, contributing to comprehensive solutions for electronic testing and validation. Collaborative efforts between academia and industry stakeholders can foster innovation and drive the adoption of cutting-edge technologies, ultimately advancing the state-of-the-art in Built-in Self-Test and electronic system reliability.

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